CLAIMS

Sub A7

1. A data receiving unit for receiving data transmissions in which data is transmitted in parallel over a plurality of conductors and a forwarded clock signal, synchronized with the data, is received over a further conductor, said unit comprising:

a. an input latch connected to receiving the data on said data conductors, said latch being clocked by alternate transitions of said forwarded clock check signal,

b. means for maintaining a delayed replica of said forwarded clock signal in synchronism with said forwarded clock signal, said delayed replica being a local clock signal for internal operations of said receiving unit,

c. a second latch connected to receive the contents of said input latch, said second latch being clocked by said local clock signal on transitions alternate to those on which said input latch is clocked.

2. A data receiving unit for receiving double-data-rate transmissions in which data is transmitted in parallel over a plurality of conductors and a forwarded clock signal, synchronized with the data, is received over a further conductor, said unit comprising:

a. first and second input latches connected to receive the data on said data conductors, said latch as being clocked by alternate transitions of said forwarded clock signal,

b. means for maintaining a delayed replica of said forwarded clock signal in synchronism with said forwarded clock signal, said delayed replica being a local clock signal for internal operations of said receiving unit,

c. the third and forth latches connected to receive the contents of said first and second input latches, respectively, said third and forth latches being clocked the same transitions of said local clock signal.

3. The receiving unit defined in claim 2 in which said first and third latches are clocked by corresponding clock edges and further including a delay element disposed in the data path from said first latch to said third latch, thereby to prevent jitter in the relative phase of the clock signals applied to said first and third latches from causing errors in the transfer of data from said first latch to said third latch.

4. The data receiving unit defined in claim 3 in which said synchronism maintaining means synchronizes said delayed replica with the forwarded clock signal as received at said first latch.

5. The receiving unit defined in claim 4 in which said local clock signal is delayed relative to the forwarded clock signal by an interval that is substantially equal to the time required for the local clock signal to reach components in said receiving unit clocked by that signal.

Add A6)